# NTR4502P, NVTR4502P

# Power MOSFET

## −30 V, −1.95 A, Single, P−Channel, SOT−23

**ON Semiconductor®**

**http://onsemi.com**

| $V_{(BR)DSS}$ | $R_{DS(on)}$ TYP | $I_D$ Max (Note 1) |
|---|---|---|
| −30 V | 155 mΩ @ −10 V | −1.95 A |
| | 240 mΩ @ −4.5 V | |

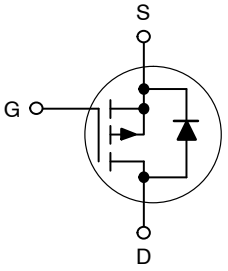
### Features

- Leading Planar Technology for Low Gate Charge / Fast Switching
- Low $R_{DS(ON)}$ for Low Conduction Losses
- SOT−23 Surface Mount for Small Footprint (3 X 3 mm)
- AEC Q101 Qualified − NVTR4502P
- These Devices are Pb−Free and are RoHS Compliant

### Applications

- DC to DC Conversion
- Load/Power Switch for Portables and Computing
- Motherboard, Notebooks, Camcorders, Digital Camera's, etc.
- Battery Charging Circuits

**P−Channel MOSFET**




**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise stated)

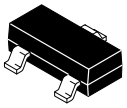
| Parameter | | | Symbol | Value | Unit |
|---|---|---|---|---|---|
| Drain−to−Source Voltage | | | $V_{DSS}$ | −30 | V |
| Gate−to−Source Voltage | | | $V_{GS}$ | ±20 | V |
| Drain Current (Note 1) | t < 10 s | $T_A$ = 25°C | $I_D$ | −1.95 | A |
| | | $T_A$ = 70°C | | −1.56 | |
| Power Dissipation (Note 1) | t < 10 s | | $P_D$ | 1.25 | W |
| Continuous Drain Current (Note 1) | Steady State | $T_A$ = 25°C | $I_D$ | −1.13 | A |
| | | $T_A$ = 70°C | | −0.90 | |
| Power Dissipation (Note 1) | Steady State | | $P_D$ | 0.4 | W |
| Pulsed Drain Current | $t_p$ = 10 μs | | $I_{DM}$ | −6.8 | A |
| Operating Junction and Storage Temperature | | | $T_J$, $T_{STG}$ | −55 to 150 | °C |
| Source Current (Body Diode) | | | $I_S$ | −1.25 | A |
| Lead Temperature for Soldering Purposes (1/8 in from case for 10 s) | | | $T_L$ | 260 | °C |

**THERMAL RESISTANCE RATINGS**

| Parameter | Symbol | Max | Unit |
|---|---|---|---|
| Junction−to−Ambient − Steady State (Note 1) | $R_{\theta JA}$ | 300 | °C/W |
| Junction−to−Ambient − t = 10 s (Note 1) | $R_{\theta JA}$ | 100 | |

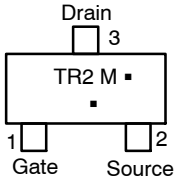
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface−mounted on FR4 board using 1 in sq. pad size (Cu area = 1.127 in sq. [1 oz] including traces).



**SOT−23**
**CASE 318**
**STYLE 21**

**MARKING DIAGRAM/ PIN ASSIGNMENT**




TR2 = Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or overbar may vary depending upon manufacturing location.

**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| NTR4502PT1G | SOT−23 (Pb−Free) | 3000 / Tape & Reel |
| NVTR4502PT1G | SOT−23 (Pb−Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

**Electrical Characteristics** ($T_J$ = 25°C unless otherwise specified)

| Parameter | Symbol | Test Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| Drain−to−Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS}$ = 0 V, $I_D$ = −250 μA | | −30 | | | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{GS}$ = 0 V, $V_{DS}$ = −30 V | $T_J$ = 25°C | | | −1 | μA |
| | | | $T_J$ = 55°C | | | −10 | |
| Gate−to−Source Leakage Current | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ±20 V | | | | ±100 | nA |
| **ON CHARACTERISTICS** (Note 3) | | | | | | | |
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{GS}$ = $V_{DS}$, $I_D$ = −250 μA | | −1.0 | | −3.0 | V |
| Drain−to−Source On Resistance | $R_{DS(on)}$ | $V_{GS}$ = −10 V, $I_D$ = −1.95 A | | | 155 | 200 | mΩ |
| | | $V_{GS}$ = −4.5 V, $I_D$ = −1.5 A | | | 240 | 350 | |
| Forward Transconductance | $g_{FS}$ | $V_{DS}$ = −10 V, $I_D$=−1.25 A | | | 3 | | S |
| **CHARGES AND CAPACITANCES** | | | | | | | |
| Input Capacitance | $C_{ISS}$ | $V_{GS}$ = 0 V, f = 1 MHz, $V_{DS}$ = −15 V | | | 200 | | pF |
| Output Capacitance | $C_{OSS}$ | | | | 80 | | |
| Reverse Transfer Capacitance | $C_{RSS}$ | | | | 50 | | |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS}$ = −10 V, $V_{DS}$ = −15 V; $I_D$ = −1.95 A | | | 6 | 10 | nC |
| Threshold Gate Charge | $Q_{G(TH)}$ | | | | 0.3 | | |
| Gate−to−Source Charge | $Q_{GS}$ | | | | 1 | | |
| Gate−to−Drain Charge | $Q_{GD}$ | | | | 1.7 | | |
| **SWITCHING CHARACTERISTICS** (Note 4) | | | | | | | |
| Turn−On Delay Time | $t_{d(ON)}$ | $V_{GS}$ =−10 V, $V_{DD}$ = −15 V, $I_D$ = −1.95 A, $R_G$ = 6 Ω | | | 5.2 | 10 | ns |
| Rise Time | $t_r$ | | | | 12 | 20 | |
| Turn−Off Delay Time | $t_{d(OFF)}$ | | | | 19 | 35 | |
| Fall Time | $t_f$ | | | | 17.5 | 30 | |
| **DRAIN−SOURCE DIODE CHARACTERISTICS** (Note 3) | | | | | | | |
| Forward Diode Voltage | $V_{SD}$ | $V_{GS}$ = 0 V, $I_S$ = −1.25 A | | | −0.8 | −1.2 | V |
| Reverse Recovery Time | $t_{RR}$ | $V_{GS}$ = 0 V, $dI_{SD}/d_t$ = 100 A/μs, $I_S$ = −1.25 A | | | 23 | | ns |

2. Surface−mounted on FR4 board using 1 in sq. pad size (Cu area = 1.127 in sq. [1 oz] including traces).
3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

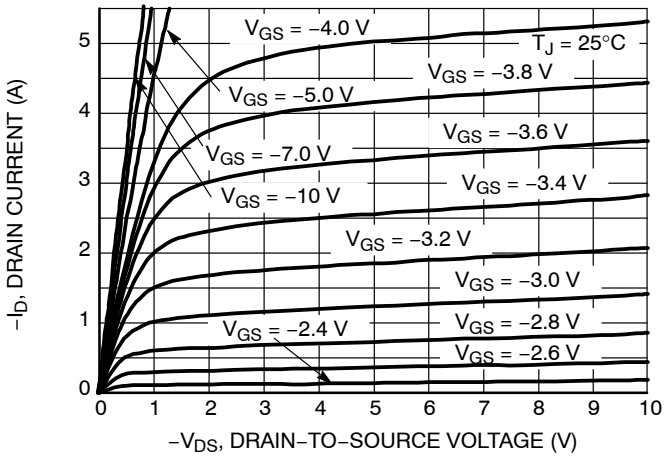



**Figure 1. On−Region Characteristics**

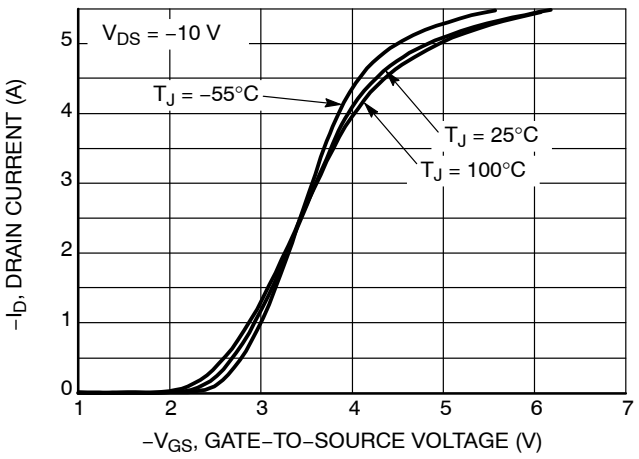



**Figure 2. Transfer Characteristics**

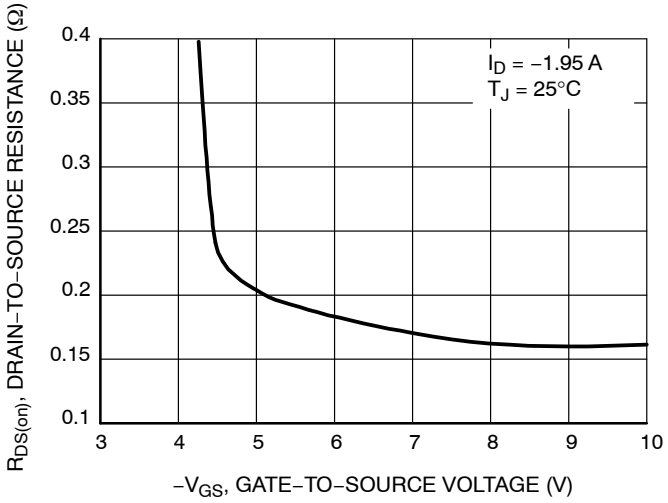



**Figure 3. On−Resistance versus Gate−to−Source Voltage**

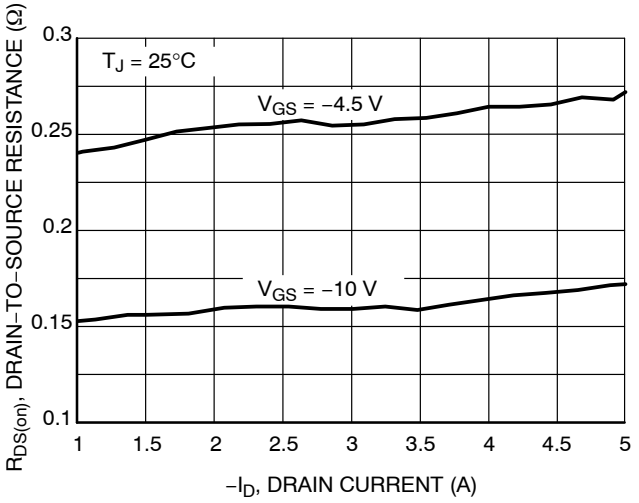



**Figure 4. On−Resistance versus Drain Current and Gate Voltage**

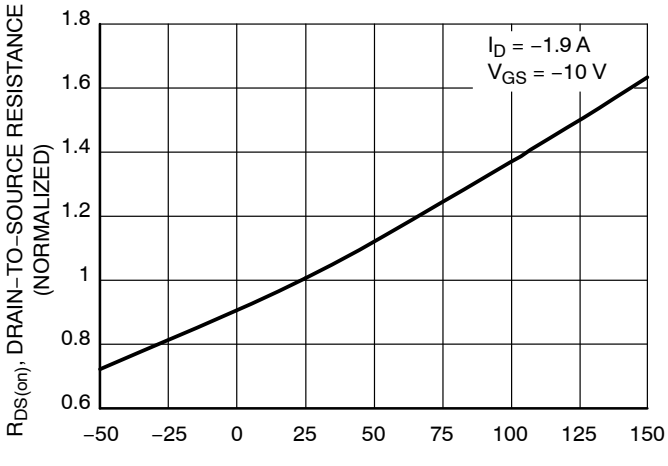



**Figure 5. On−Resistance Variation with Temperature**

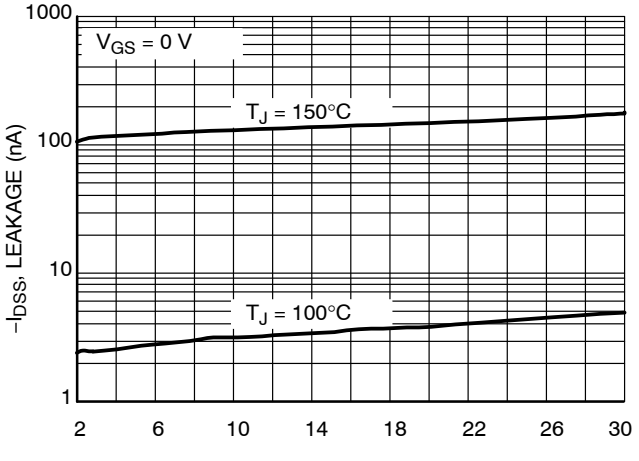



**Figure 6. Drain−to−Source Leakage Current versus Voltage**

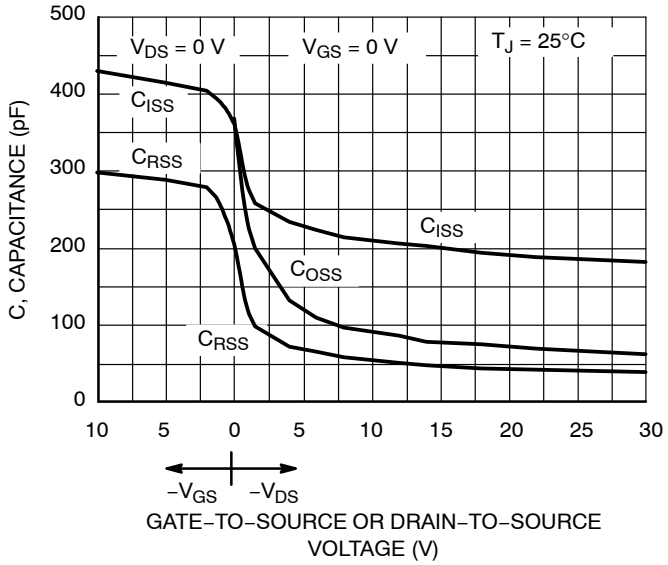



**Figure 7. Capacitance Variation**

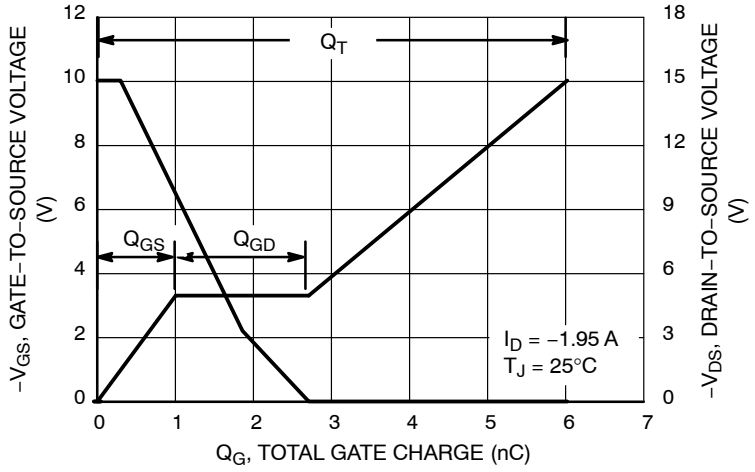



**Figure 8. Gate−to−Source and Drain−to−Source Voltage versus Total Charge**

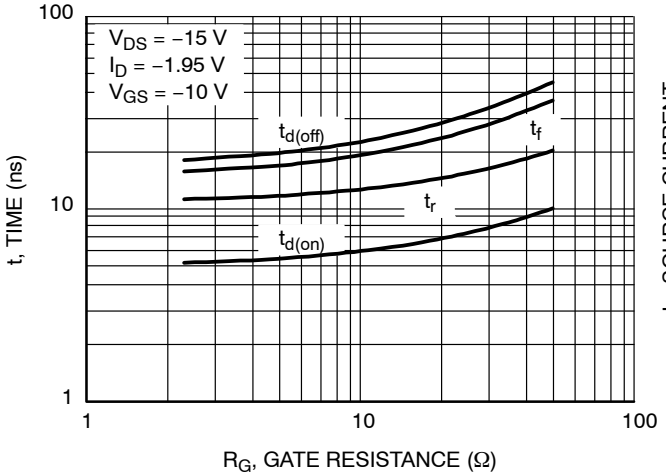



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

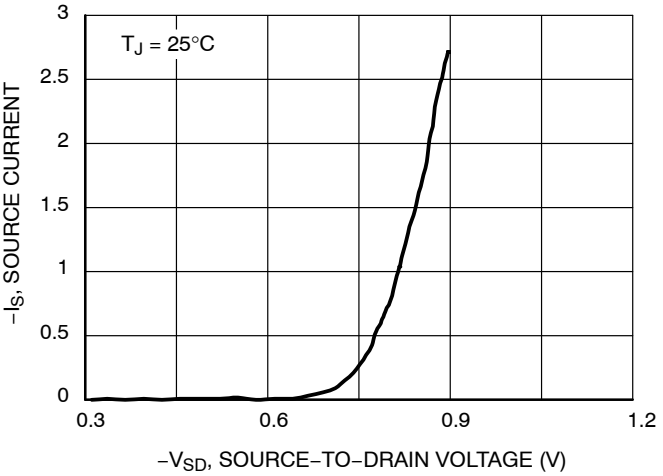
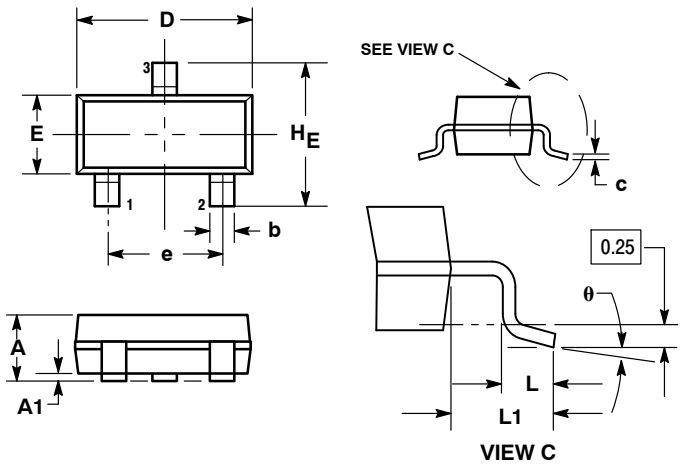



**Figure 10. Diode Forward Voltage versus Current**

## PACKAGE DIMENSIONS

**SOT−23 (TO−236)**
CASE 318−08
ISSUE AP

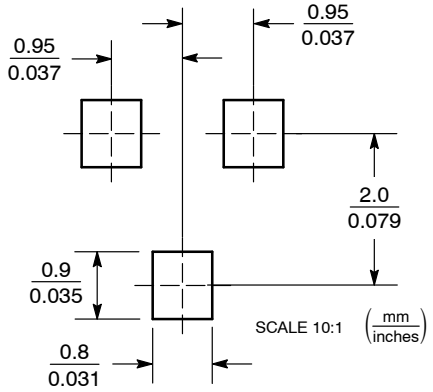



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

| | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| DIM | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.89 | 1.00 | 1.11 | 0.035 | 0.040 | 0.044 |
| A1 | 0.01 | 0.06 | 0.10 | 0.001 | 0.002 | 0.004 |
| b | 0.37 | 0.44 | 0.50 | 0.015 | 0.018 | 0.020 |
| c | 0.09 | 0.13 | 0.18 | 0.003 | 0.005 | 0.007 |
| D | 2.80 | 2.90 | 3.04 | 0.110 | 0.114 | 0.120 |
| E | 1.20 | 1.30 | 1.40 | 0.047 | 0.051 | 0.055 |
| e | 1.78 | 1.90 | 2.04 | 0.070 | 0.075 | 0.081 |
| L | 0.10 | 0.20 | 0.30 | 0.004 | 0.008 | 0.012 |
| L1 | 0.35 | 0.54 | 0.69 | 0.014 | 0.021 | 0.029 |
| $H_E$ | 2.10 | 2.40 | 2.64 | 0.083 | 0.094 | 0.104 |
| θ | 0° | −−− | 10° | 0° | −−− | 10° |

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

### SOLDERING FOOTPRINT*




*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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