

# HEF4060B

## 14-stage ripple-carry binary counter/divider and oscillator

Rev. 7 — 16 November 2011

Product data sheet

### 1. General description

The HEF4060B is a 14-stage ripple-carry binary counter/divider and oscillator with three oscillator terminals (RS, REXT and CEXT), ten buffered outputs (Q3 to Q9 and Q11 to Q13) and an overriding asynchronous master reset input (MR).

The oscillator configuration allows design of either RC or crystal oscillator circuits. The oscillator may be replaced by an external clock signal at input RS. The clock input's Schmitt-trigger action makes it highly tolerant to slower clock rise and fall times. The counter advances on the negative-going transition of RS. A HIGH level on MR resets the counter (Q3 to Q9 and Q11 to Q13 = LOW), independent of other input conditions.

It operates over a recommended  $V_{DD}$  power supply range of 3 V to 15 V referenced to  $V_{SS}$  (usually ground). Unused inputs must be connected to  $V_{DD}$ ,  $V_{SS}$ , or another input.

### 2. Features and benefits

- Tolerant of slow clock rise and fall times
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Inputs and outputs are protected against electrostatic effects
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$
- Complies with JEDEC standard JESD 13-B

### 3. Ordering information

**Table 1. Ordering information**

All types operate from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ .

Type number	Package		Version
	Name	Description	
HEF4060BP	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
HEF4060BT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1



### 4. Functional diagram

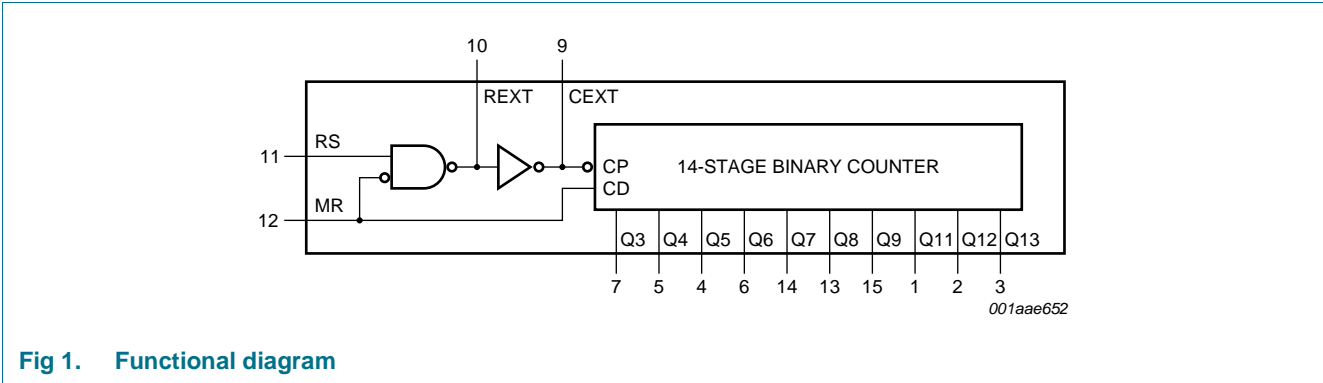


Fig 1. Functional diagram

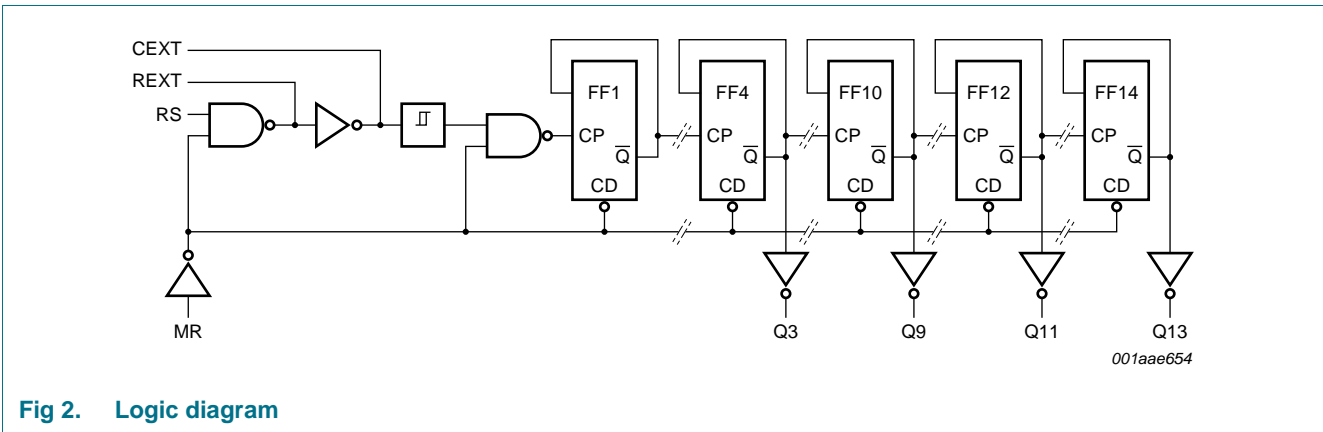


Fig 2. Logic diagram

### 5. Pinning information

#### 5.1 Pinning

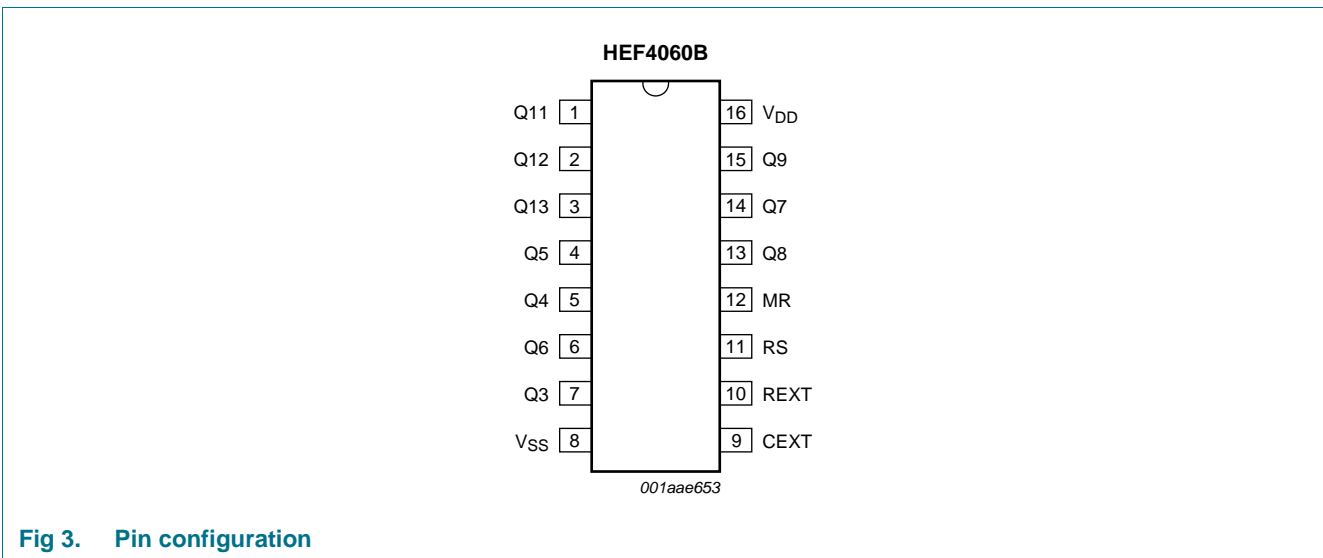


Fig 3. Pin configuration

## 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
Q11 to Q13	1, 2, 3	counter output
Q3 to Q9	7, 5, 4, 6, 14, 13, 15	counter output
V <sub>SS</sub>	8	ground supply voltage
CEXT	9	external capacitor connection
REXT	10	oscillator pin
RS	11	clock input/oscillator pin
MR	12	master reset
V <sub>DD</sub>	16	supply voltage

## 6. Functional description

Table 3. Function table<sup>[1]</sup>

Input		Output
RS	MR	Q3 to Q9 and Q11 to Q13
↑	L	no change
↓	L	count
X	H	L

[1] H = HIGH voltage level; L = LOW voltage level; ↑ = LOW-to-HIGH clock transition; ↓ HIGH-to-LOW clock transition.

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
V <sub>DD</sub>	supply voltage		-0.5	+18	V	
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>DD</sub> + 0.5 V	-	±10	mA	
V <sub>I</sub>	input voltage		-0.5	V <sub>DD</sub> + 0.5	V	
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>DD</sub> + 0.5 V	-	±10	mA	
I <sub>I/O</sub>	input/output current		-	±10	mA	
I <sub>DD</sub>	supply current		-	50	mA	
T <sub>stg</sub>	storage temperature		-65	+150	°C	
T <sub>amb</sub>	ambient temperature		-40	+85	°C	
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> -40 °C to +85 °C				
		DIP16 package	[1]	-	750	mW
		SO16 package	[2]	-	500	mW
P	power dissipation	per output	-	100	mW	

[1] For DIP16 package: P<sub>tot</sub> derates linearly with 12 mW/K above 70 °C.

[2] For SO16 package: P<sub>tot</sub> derates linearly with 8 mW/K above 70 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD}$	supply voltage		3	-	15	V
$V_I$	input voltage		0	-	$V_{DD}$	V
$T_{amb}$	ambient temperature	in free air	-40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	input MR				
		$V_{DD} = 5\text{ V}$	-	-	3.75	$\mu\text{s/V}$
		$V_{DD} = 10\text{ V}$	-	-	0.5	$\mu\text{s/V}$
		$V_{DD} = 15\text{ V}$	-	-	0.08	$\mu\text{s/V}$

## 9. Static characteristics

**Table 6. Static characteristics**

$V_{SS} = 0\text{ V}$ ;  $V_I = V_{SS}$  or  $V_{DD}$  unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	$T_{amb} = -40\text{ °C}$		$T_{amb} = 25\text{ °C}$		$T_{amb} = 85\text{ °C}$		Unit
				Min	Max	Min	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$ I_O  < 1\ \mu\text{A}$	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
$V_{IL}$	LOW-level input voltage	$ I_O  < 1\ \mu\text{A}$	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
$V_{OH}$	HIGH-level output voltage	$ I_O  < 1\ \mu\text{A}$	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
$V_{OL}$	LOW-level output voltage	$ I_O  < 1\ \mu\text{A}$	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
$I_{OH}$	HIGH-level output current	$V_O = 2.5\text{ V}$	5 V	-	-1.7	-	-1.4	-	-1.1	mA
		$V_O = 4.6\text{ V}$	5 V	-	-0.52	-	-0.44	-	-0.36	mA
		$V_O = 9.5\text{ V}$	10 V	-	-1.3	-	-1.1	-	-0.9	mA
		$V_O = 13.5\text{ V}$	15 V	-	-3.6	-	-3.0	-	-2.4	mA
$I_{OL}$	LOW-level output current	$V_O = 0.4\text{ V}$	5 V	0.52	-	0.44	-	0.36	-	mA
		$V_O = 0.5\text{ V}$	10 V	1.3	-	1.1	-	0.9	-	mA
		$V_O = 1.5\text{ V}$	15 V	3.6	-	3.0	-	2.4	-	mA
$I_I$	input leakage current		15 V	-	$\pm 0.3$	-	$\pm 0.3$	-	$\pm 1.0$	$\mu\text{A}$
$I_{DD}$	supply current	$I_O = 0\text{ A}$	5 V	-	20	-	20	-	150	$\mu\text{A}$
			10 V	-	40	-	40	-	300	$\mu\text{A}$
			15 V	-	80	-	80	-	600	$\mu\text{A}$
$C_I$	input capacitance		-	-	-	-	7.5	-	-	pF

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

$T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $V_{SS} = 0\text{ V}$ ;  $C_L = 50\text{ pF}$ ;  $t_r = t_f \leq 20\text{ ns}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	Extrapolation formula <sup>[1]</sup>	Min	Typ	Max	Unit
$t_{pd}$	propagation delay	RS $\rightarrow$ Q3; see <a href="#">Figure 4</a>	5 V <sup>[2]</sup>	$183\text{ ns} + (0.55\text{ ns/pF}) C_L$	-	210	420	ns
			10 V	$69\text{ ns} + (0.23\text{ ns/pF}) C_L$	-	80	160	ns
			15 V	$42\text{ ns} + (0.16\text{ ns/pF}) C_L$	-	50	100	ns
		Qn $\rightarrow$ Qn + 1; see <a href="#">Figure 4</a>	5 V	-	-	25	50	ns
			10 V	-	-	10	20	ns
			15 V	-	-	6	12	ns
		MR $\rightarrow$ Qn; HIGH to LOW see <a href="#">Figure 4</a>	5 V	$73\text{ ns} + (0.55\text{ ns/pF}) C_L$	-	100	200	ns
			10 V	$29\text{ ns} + (0.23\text{ ns/pF}) C_L$	-	40	80	ns
			15 V	$22\text{ ns} + (0.16\text{ ns/pF}) C_L$	-	30	60	ns
$t_t$	transition time	see <a href="#">Figure 4</a>	5 V <sup>[3]</sup>	$10\text{ ns} + (1.00\text{ ns/pF}) C_L$	-	60	120	ns
			10 V	$9\text{ ns} + (0.42\text{ ns/pF}) C_L$	-	30	60	ns
			15 V	$6\text{ ns} + (0.28\text{ ns/pF}) C_L$	-	20	40	ns
$t_w$	pulse width	minimum width; RS HIGH; see <a href="#">Figure 4</a>	5 V	-	120	60	-	ns
			10 V	-	50	25	-	ns
			15 V	-	30	15	-	ns
		minimum width; MR HIGH; see <a href="#">Figure 4</a>	5 V	-	50	25	-	ns
			10 V	-	30	15	-	ns
			15 V	-	20	10	-	ns
$t_{rec}$	recovery time	input MR; see <a href="#">Figure 4</a>	5 V	-	160	80	-	ns
			10 V	-	80	40	-	ns
			15 V	-	60	30	-	ns
$f_{max}$	maximum frequency	input RS; see <a href="#">Figure 4</a>	5 V	-	4	8	-	MHz
			10 V	-	10	20	-	MHz
			15 V	-	15	30	-	MHz

[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown ( $C_L$  in pF).

[2]  $t_{pd}$  is the same as  $t_{PHL}$  and  $t_{PLH}$ .

[3]  $t_t$  is the same as  $t_{THL}$  and  $t_{TLH}$ .

**Table 8. Power dissipation**

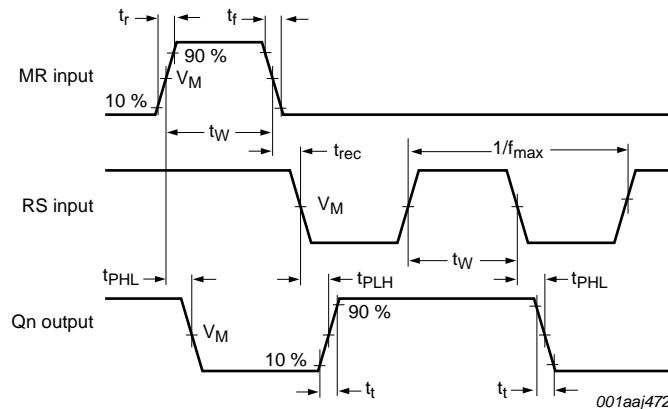
Dynamic power dissipation  $P_D$  and total power dissipation  $P_{tot}$  can be calculated from the formulas shown.  $T_{amb} = 25\text{ }^\circ\text{C}$ .

Symbol	Parameter	Conditions	$V_{DD}$	Typical formula for $P_D$ and $P_{tot}$ ( $\mu\text{W}$ ) <sup>[1]</sup>
$P_D$	dynamic power dissipation	per device	5 V	$P_D = 700 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$
			10 V	$P_D = 3300 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$
			15 V	$P_D = 8900 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$
$P_{tot}$	total power dissipation	when using the on-chip oscillator	5 V	$P_{tot} = 700 \times f_{osc} + \Sigma(f_o \times C_L) \times V_{DD}^2 + 2 \times C_t \times V_{DD}^2 \times f_{osc} + 690 \times V_{DD}$
			10 V	$P_{tot} = 3300 \times f_{osc} + \Sigma(f_o \times C_L) \times V_{DD}^2 + 2 \times C_t \times V_{DD}^2 \times f_{osc} + 6900 \times V_{DD}$
			15 V	$P_{tot} = 8900 \times f_{osc} + \Sigma(f_o \times C_L) \times V_{DD}^2 + 2 \times C_t \times V_{DD}^2 \times f_{osc} + 22000 \times V_{DD}$

[1] Where:

- $f_i$  = input frequency in MHz;  $f_o$  = output frequency in MHz;
- $C_L$  = output load capacitance in pF;
- $V_{DD}$  = supply voltage in V;
- $\Sigma(f_o \times C_L)$  = sum of the outputs;
- $C_t$  = timing capacitance (pF);
- $f_{osc}$  = oscillator frequency (MHz).

## 11. Waveforms

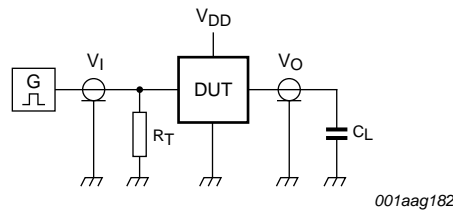


Measurement points are given in [Table 9](#).

**Fig 4. Waveforms showing propagation delays for MR to Qn and  $\overline{CP}$  to Q0, minimum MR, and  $\overline{CP}$  pulse widths**

**Table 9. Measurement points**

Supply voltage	Input	Output
$V_{DD}$	$V_M$	$V_M$
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$



Test data is given in [Table 10](#).

Definitions for test circuit:

DUT = Device Under Test;

$C_L$  = load capacitance including jig and probe capacitance;

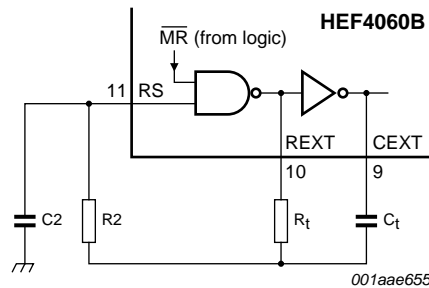
$R_T$  = termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

**Fig 5. Test circuit for switching times**

**Table 10. Measurement point and test data**

Supply voltage	Input		Load
$V_{DD}$	$V_I$	$t_r, t_f$	$C_L$
5 V to 15 V	$V_{SS}$ or $V_{DD}$	$\leq 20$ ns	50 pF

## 12. RC oscillator



Typical formula for oscillator frequency: 
$$f_{osc} = \frac{1}{2.3 \times R_t \times C_t}$$

**Fig 6. External component connection for RC oscillator**

### 12.1 Timing component limitations

The oscillator frequency is mainly determined by  $R_t \times C_t$ , provided  $R_t \ll R_2$  and  $R_2 \times C_2 \ll R_t \times C_t$ . The influence of the forward voltage across the input protection diodes on the frequency is minimized by  $R_2$ . The stray capacitance  $C_2$  should be kept as small as possible. In consideration of accuracy,  $C_t$  must be larger than the inherent stray capacitance.  $R_t$  must be larger than the LOCMOS (Local Oxidation Complementary Metal-Oxide Semiconductor) 'ON' resistance in series with it, which typically is 500  $\Omega$  at  $V_{DD} = 5$  V, 300  $\Omega$  at  $V_{DD} = 10$  V and 200  $\Omega$  at  $V_{DD} = 15$  V.

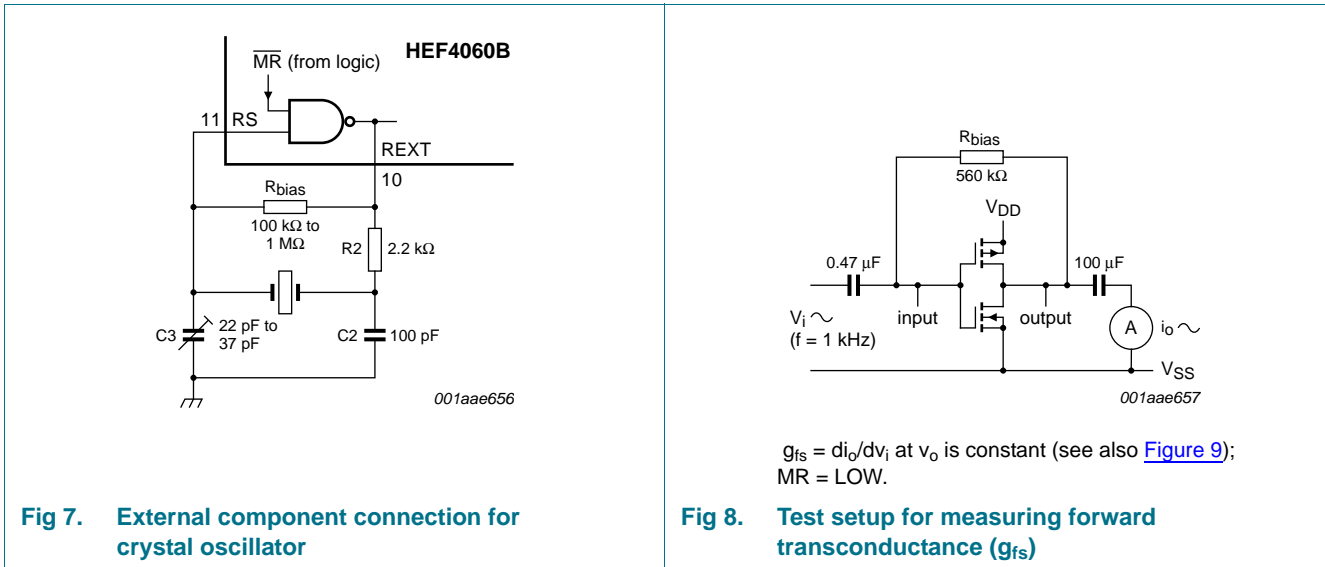
The recommended values for these components to maintain agreement with the typical oscillation formula are:

$$C_t \geq 100 \text{ pF, up to any practical value,}$$

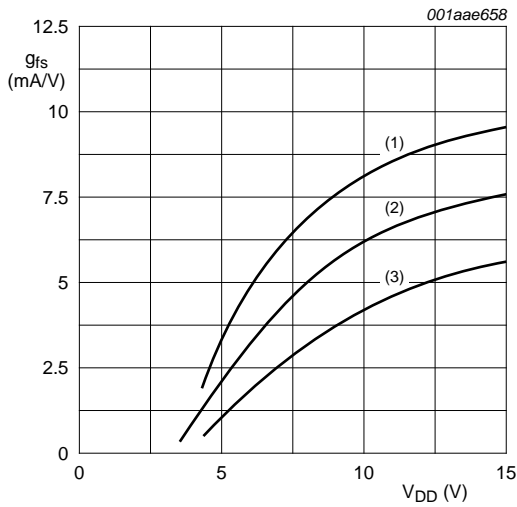
$$10 \text{ k}\Omega \leq R_t \leq 1 \text{ M}\Omega.$$

### 12.2 Typical crystal oscillator circuit

In [Figure 7](#), R2 is the power limiting resistor. For starting and maintaining oscillation a minimum transconductance is necessary.

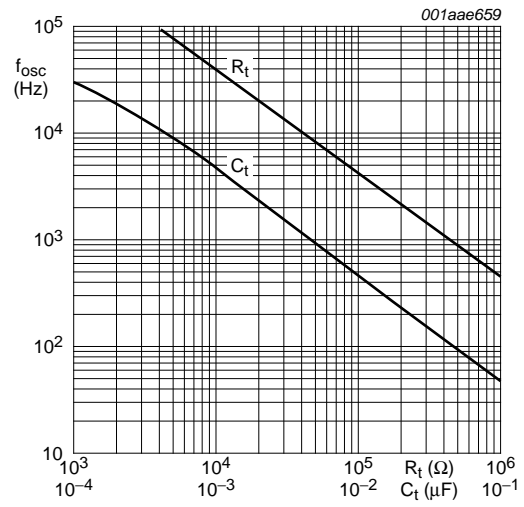






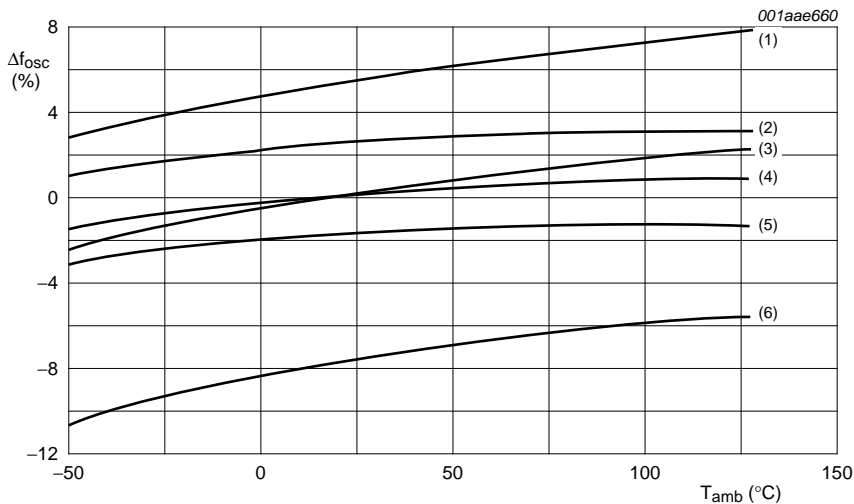
$T_{amb} = 25\text{ }^{\circ}\text{C}$ .  
 (1) Average +  $2\sigma$ .  
 (2) Average.  
 (3) Average -  $2\sigma$ .  
 Where ' $\sigma$ ' is the observed standard deviation.

**Fig 9. Typical forward transconductance  $g_{fs}$  as a function of the supply voltage**



$C_t$  curve at  $R_t = 100\text{ k}\Omega$ ;  $R_2 = 470\text{ k}\Omega$ .  
 $R_t$  curve at  $C_t = 1\text{ nF}$ ;  $R_2 = 5 R_t$ .  
 $V_{DD} = 5\text{ V to } 15\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

**Fig 10. RC oscillator frequency as a function of  $R_t$  and  $C_t$**



Lines (1) and (2):  $V_{DD} = 15\text{ V}$ .  
 Lines (3) and (4):  $V_{DD} = 10\text{ V}$ .  
 Lines (5) and (6):  $V_{DD} = 5\text{ V}$ .  
 Lines (1), (3), (6):  $R_t = 100\text{ k}\Omega$ ;  $C_t = 1\text{ nF}$ ;  $R_2 = 0\text{ W}$ .  
 Lines (2), (4), (5):  $R_t = 100\text{ k}\Omega$ ;  $C_t = 1\text{ nF}$ ;  $R_2 = 300\text{ k}\Omega$ .  
 Referenced at:  $f_{osc}$  at  $T_{amb} = 25\text{ }^{\circ}\text{C}$  and  $V_{DD} = 10\text{ V}$ .

**Fig 11. Oscillator frequency deviation ( $\Delta f_{osc}$ ) as a function of ambient temperature**

13. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4

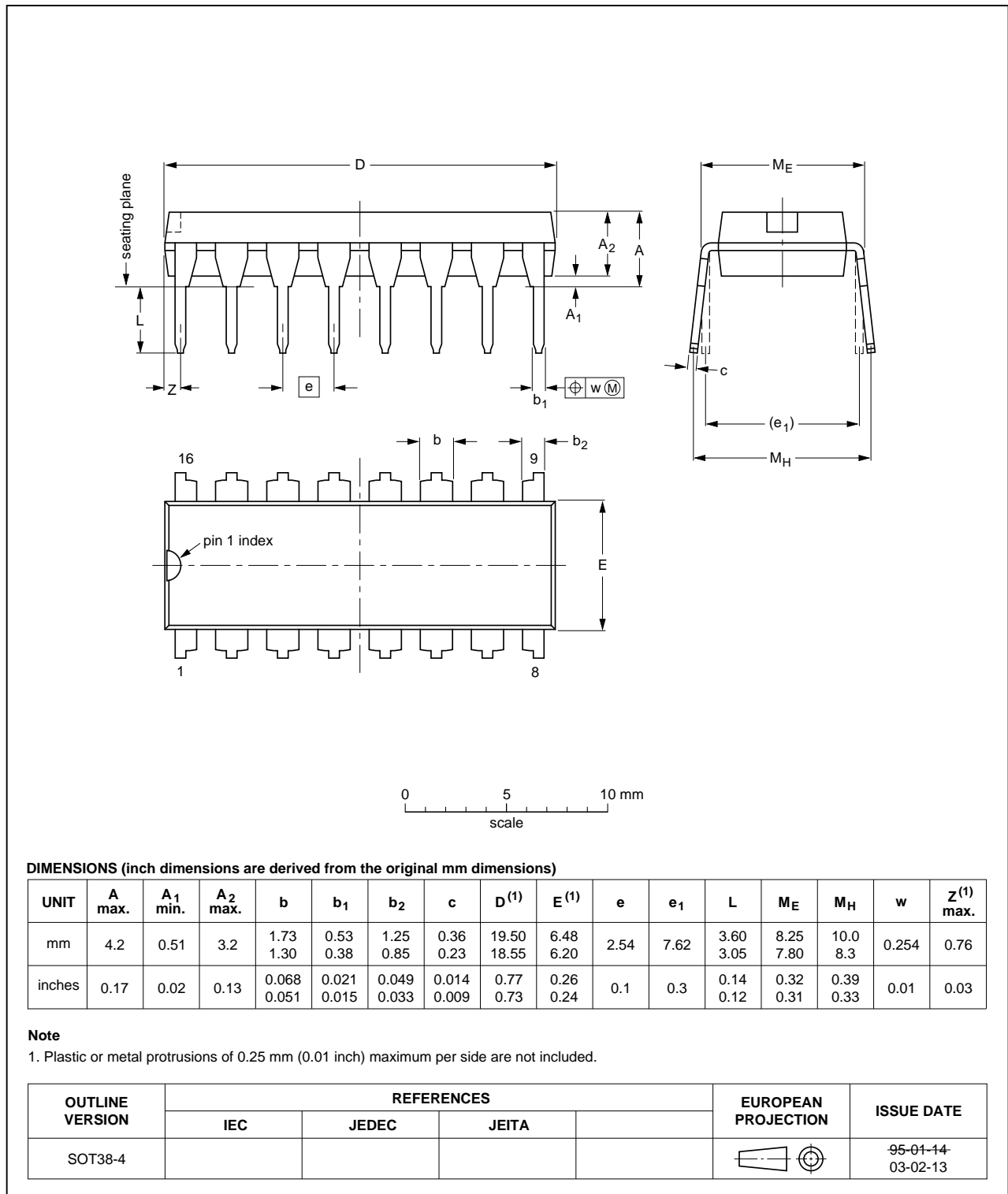


Fig 12. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

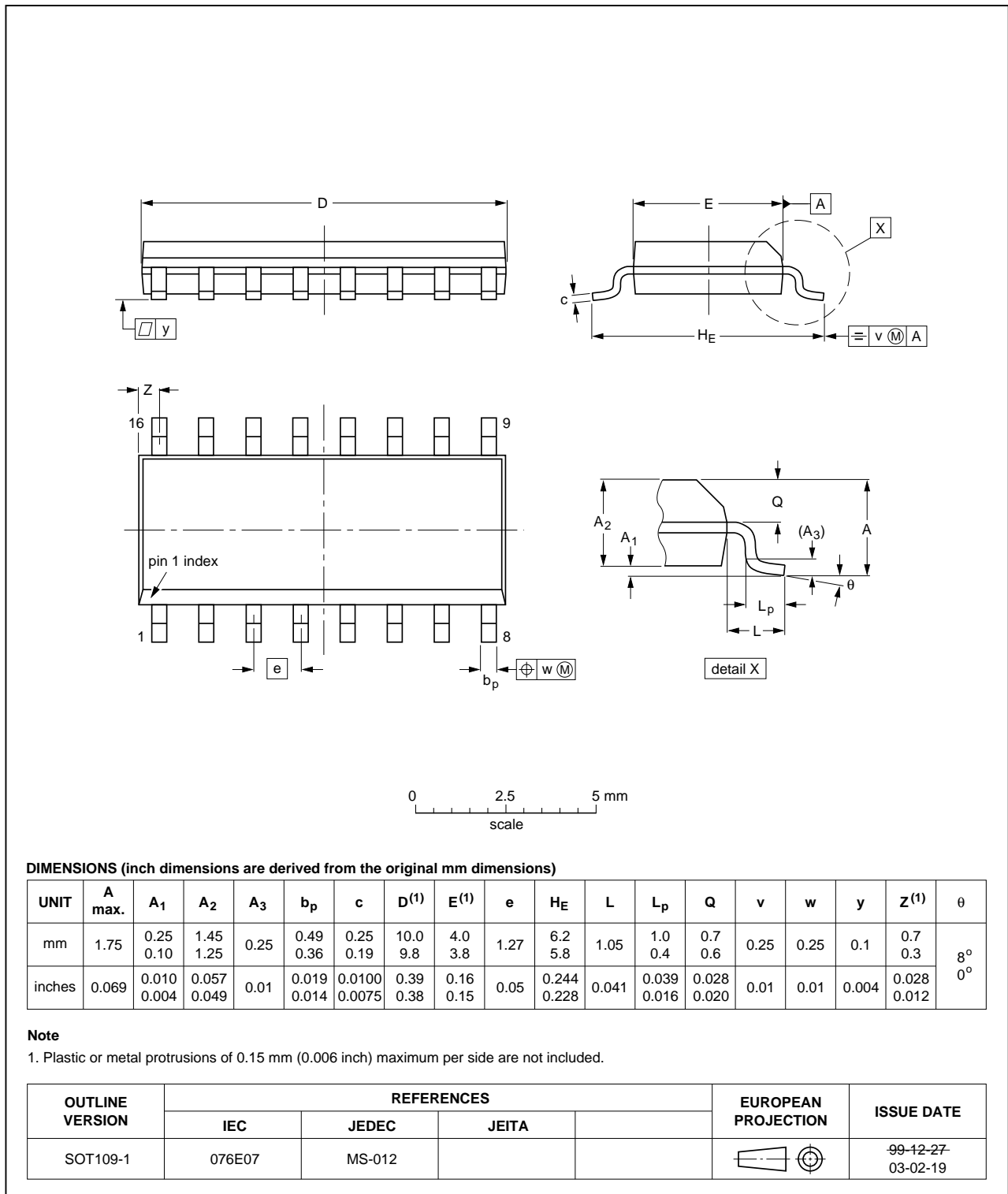


Fig 13. Package outline SOT109-1 (SO16)

## 14. Revision history

**Table 11. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4060B v.7	20111116	Product data sheet	-	HEF4060B v.6
Modifications:	<ul style="list-style-type: none"><li>• Legal pages updated.</li><li>• Changes in “General description” and “Features and benefits”.</li><li>• Section “Applications” removed.</li></ul>			
HEF4060B v.6	20110511	Product data sheet	-	HEF4060B v.5
HEF4060B v.5	20091127	Product data sheet	-	HEF4060B v.4
HEF4060B v.4	20090817	Product data sheet	-	HEF4060B_CNV v.3
HEF4060B_CNV v.3	19950101	Product specification	-	HEF4060B_CNV v.2
HEF4060B_CNV v.2	19950101	Product specification	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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