# *Voltage Detectors ,70XX Series*

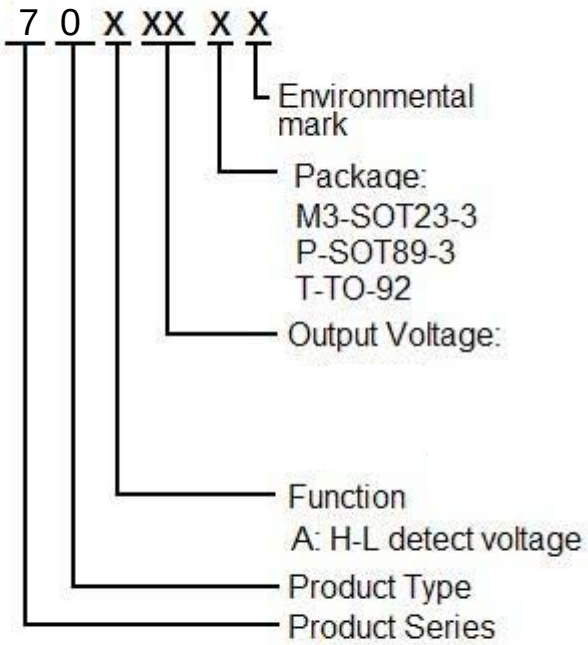
## General Description

70XX Series are a set of three-terminal low power voltage detectors implemented in NMOS technology. Each voltage detector in the series detects a particular fixed voltage ranging from 2.0V to 7.0V. The voltage detectors consist of a high precision and low power consumption standard voltage source, a comparator, hysteresis circuit, and an output driver. NMOS technology ensures low power consumption.

## Features

- Highly accuracy： ±1%
- Low power consumption：TYP 1.8uA (Vin=3V)
- Detect voltage range：2.0V~7.0V in 0.1V increments
- Operating voltage range：1.5V~18V
- Detect voltage temperature characteristics：
  TYP±0.9mV/℃
- Output configuration： NMOS
- Package： SOT-23-3，SOT-89-3，TO-92

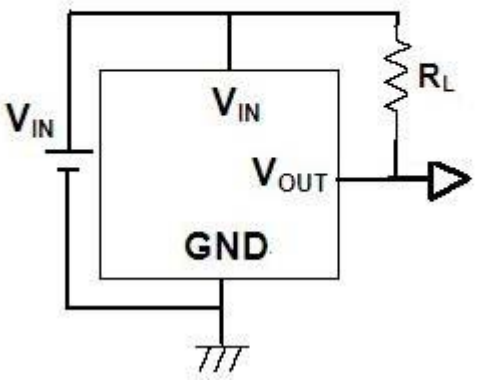
## Selection Guide




## Typical Application

- battery checkers
- Level selectors
- Power failure detectors
- Microcomputer reset
- Battery backup of Memories

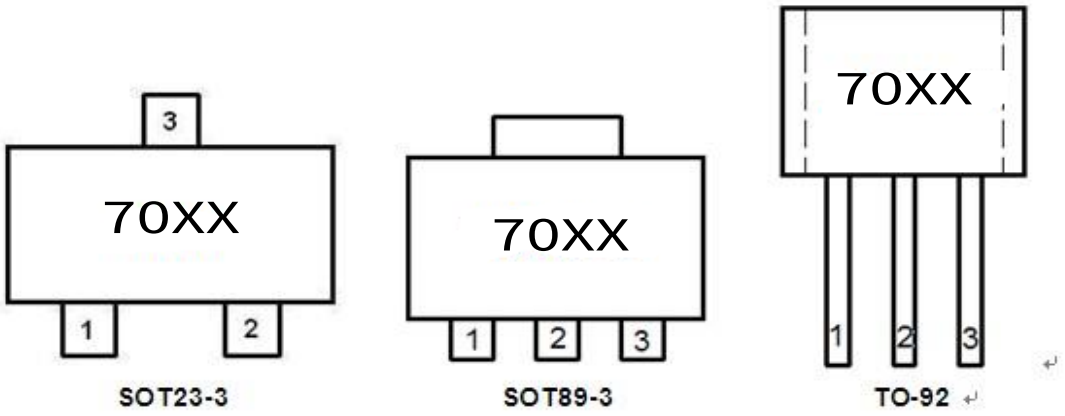
## Typical Application Circuit



**Selection Table**

| Part No. | Detectable Voltage | Hysteresis Width | Tolerance | Package | Marking |
|---|---|---|---|---|---|
| 7022 | 2.2V | 0.11V | ±2% | TO92<br>SOT89<br>SOT23-3 | 70XX(for TO92)<br>70XX(for SOT89) |
| 7024 | 2.4V | 0.12V | ±2% | | |
| 7027 | 2.7V | 0.135V | ±2% | | |
| 7033 | 3.3V | 0.165V | ±2% | | |
| 7039 | 3.9V | 0.195V | ±2% | | |
| 7044 | 4.4V | 0.22V | ±2% | | |
| 7050 | 5.0V | 0.25V | ±2% | | |

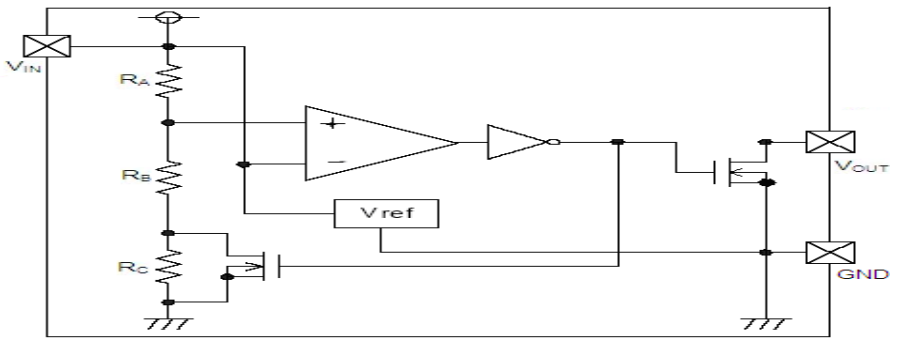
## Pin Configuration




## Pin Assignment

| Pin Number | | | Pin Name | Functions |
|---|---|---|---|---|
| SOT-23-3 | SOT-89-3 | TO-92 | | |
| 2 | 3 | 3 | GND | Ground |
| 1 | 1 | 1 | $V_{OUT}$ | Output Voltage |
| 3 | 2 | 2 | $V_{IN}$ | Input Voltage |

## Block Diagram



## Absolute Maximum Ratings

| PARAMETER | | SYMBAL | RATINGS | UNITS |
|---|---|---|---|---|
| $V_{IN}$ Input Voltage | | $V_{IN}$ | 18 | V |
| Output Current | | $I_{OUT}$ | 50 | mA |
| Output Voltage | NMOS | $V_{OUT}$ | GND-0.3~ $V_{IN}$ +0.3 | V |
| Continuous Total Power Dissipation | SOT23-3 | $P_D$ | 300 | mW |
| | SOT89-3 | | 500 | |
| | TO-92 | | 500 | |
| Operating Ambient Temperature | | $T_{Opr}$ | 0~+70 | ℃ |
| Storage Temperature | | $T_{stg}$ | -50~+125 | ℃ |
| Soldering temperature and time | | $T_{solder}$ | 260℃, 10s | |

## Electrical Characteristics ($V_{DET}$ =2.0V to 7.0V ,$T_A$=25℃ ,unless otherwise noted)

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| **$V_{DET}$** | Detect Voltage | | | $V_{DET}$×0.99 | $V_{DET}$ | $V_{DET}$×1.01 | V |
| **$V_{HYS}$** | Hysteresis Width | | | $V_{DET}$×0.02 | $V_{DET}$×0.05 | $V_{DET}$×0.1 | V |
| **$I_{IN}$** | Operating Current | $V_{DET}$=2.0V~ 2.8V | $V_{IN}$ =3.0V | - | 1.8 | 3 | μA |
| | | $V_{DET}$ =2.8V~ 3.6V | $V_{IN}$ =4.0V | - | 1.8 | 4 | |
| | | $V_{DET}$ =3.6V ~ 4.7V | $V_{IN}$ =5.0V | - | 2.1 | 4 | |
| | | $V_{DET}$ =4.7V~ 7.0V | $V_{IN}$ =8.0V | - | 2.5 | 4 | |
| **$V_{IN}$** | Operating Voltage | $V_{DET}$ =2.0V to 7.0V | | 0.7 | - | 18 | V |
| **$I_{OL}$** | Output Sink Current | $V_{DET}$=2.0V~ 2.8V | $V_{IN}$ =-$V_{DET(S)}$ -0.2 V , $V_{OUT}$=0.2V | 0.5 | | | mA |
| | | $V_{DET}$ =2.8V~ 3.6V | $V_{IN}$ =-$V_{DET(S)}$ -0.5 V , $V_{OUT}$=0.3V | 0.5 | | | |
| | | $V_{DET}$ =3.6V ~ 4.7V | $V_{IN}$ =-$V_{DET(S)}$ -0.5 V , $V_{OUT}$=0.3V | 1.2 | | | |
| | | $V_{DET}$ =4.7V~ 7.0V | $V_{IN}$ =-$V_{DET(S)}$ -0.5 V , $V_{OUT}$=0.3V | 2.5 | | | |
| **$\Delta V_{DET}/\Delta T_A$** | Temperature characteristics | 0℃≤$T_{opr}$≤70℃ | | | ±0.9 | | mV/℃ |

**Note:** Use this IC within the stated maximum ratings. Operation beyond these limits may cause degrading or permanent damage to the device.

## Functional Description

The 70xx series is a set of vo ltage detectors equipped with a high stability voltage reference which is connected to the negative input of a comparator — denoted as $V_{REF}$ in the following figure (Fig. 1).When the voltage drop to the positive input of the comparator (i,e,$V_B$) is higher than $V_{REF}$, $V_{OUT}$ goes high, M1 turns off, and $V_B$ is ex-pressed as $V_{BH}=V_{IN}\times(R_B+R_C)/(R_A+R_B+R_C)$.If $V_{IN}$ is decreased so that $V_B$ falls to a value that is less than $V_{REF}$, the comparator output inverts (from high to low), $V_{OUT}$ goes low, $V_C$ is high, M1 turns on, $R_C$ is bypassed, and $V_B$ becomes: $V_{BL}=V_{IN}\times R_B/(R_A+R_B)$, which is less than $V_{BH}$. By so doing the comparator out-put will stay low to prevent the circuit from oscillating when $V_B \approx V_{REF}$. If $V_{IN}$ falls bellow the minimum operating voltage, the output becomes undefined. When $V_{IN}$ goes from low to $V_{IN}\times R_B/(R_A+R_B) > V_{REF}$, the comparator output goes high and $V_{OUT}$ goes high again. The detection voltage is as defined:

$$V_{DET(-)}=(R_A+R_B+R_C)\times V_{REF}/(R_B+R_C)$$

The release voltage is as defined:

$$V_{DET(+)}=(R_A+R_B)\times V_{REF}/R_B$$

The hysteresis width is:

$$V_{HYS}=V_{DET(+)}-V_{DET(-)}$$

Fig.1 demonstrates the NMOS output type with positive output polarity ($V_{OUT}$ is normally high, active low).

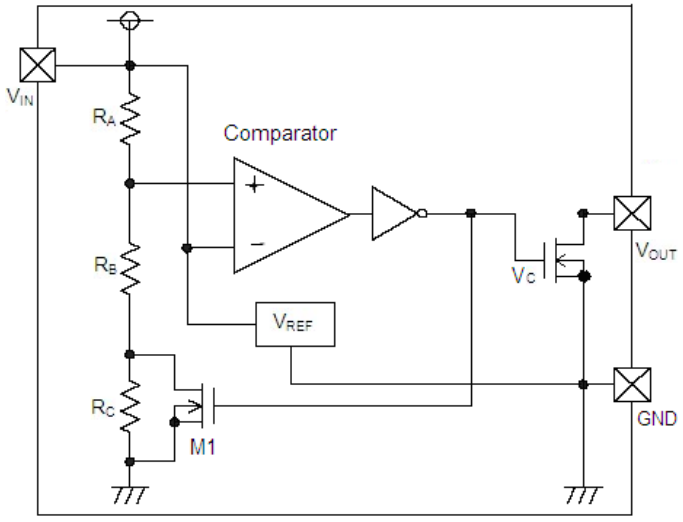
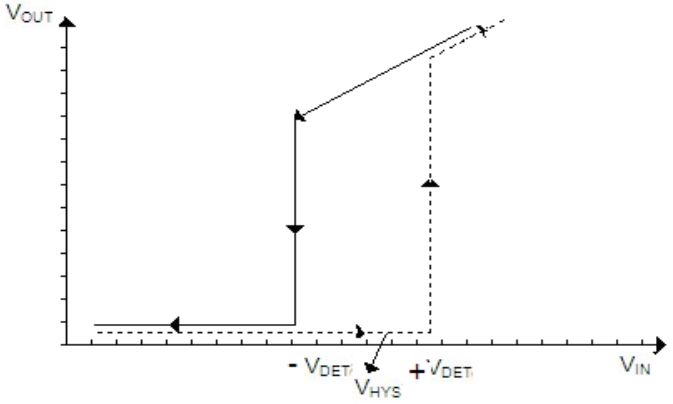


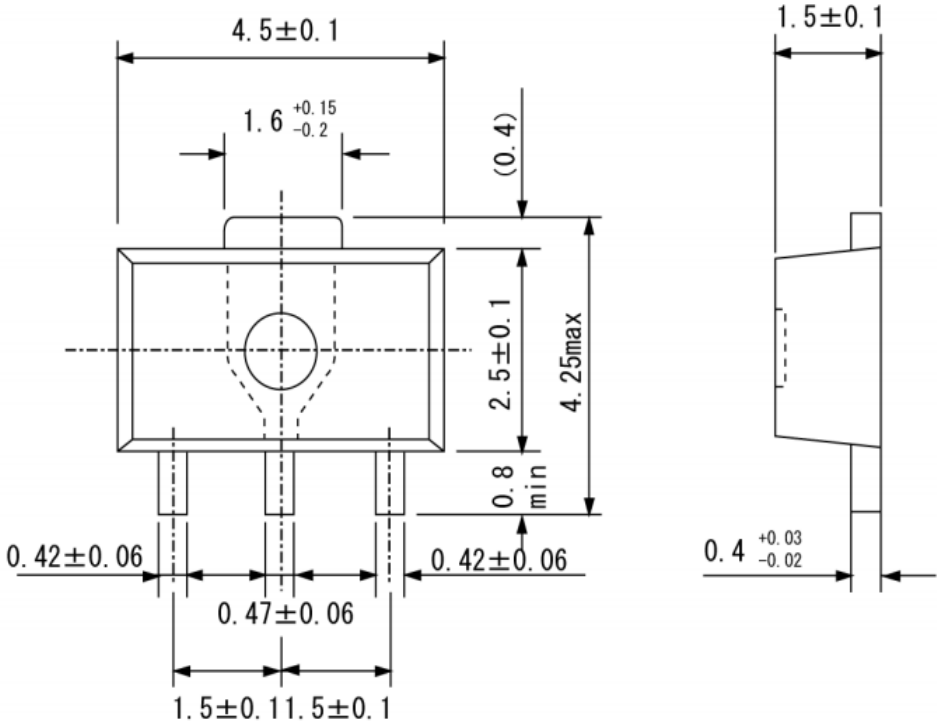

Fig.1 NMOS output volt age detector (70XX)

## Timing Chart

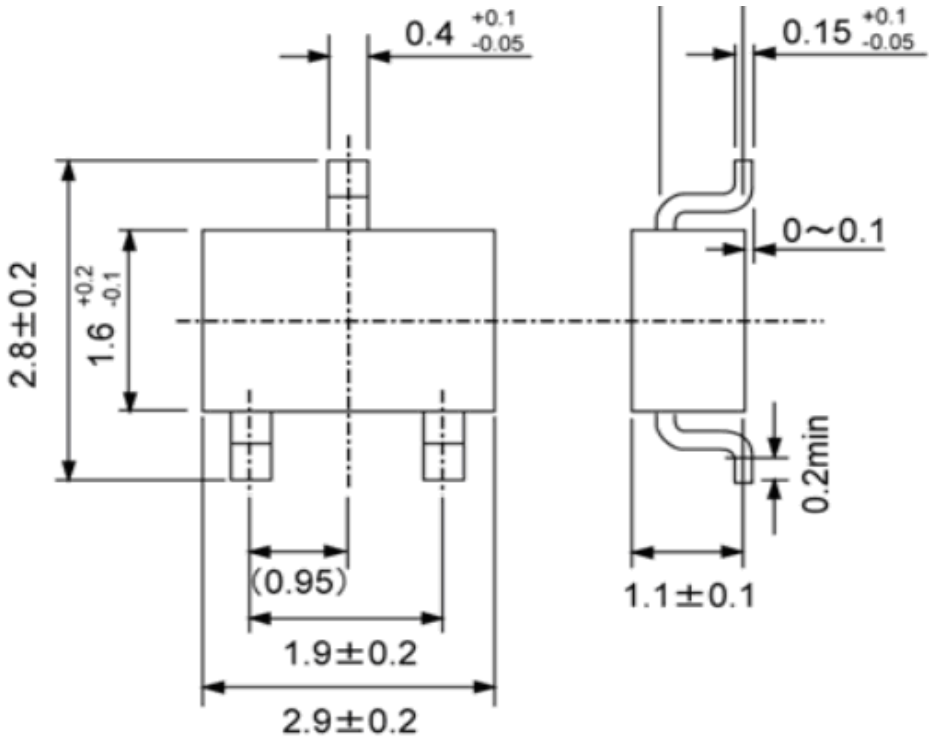


## Package Information

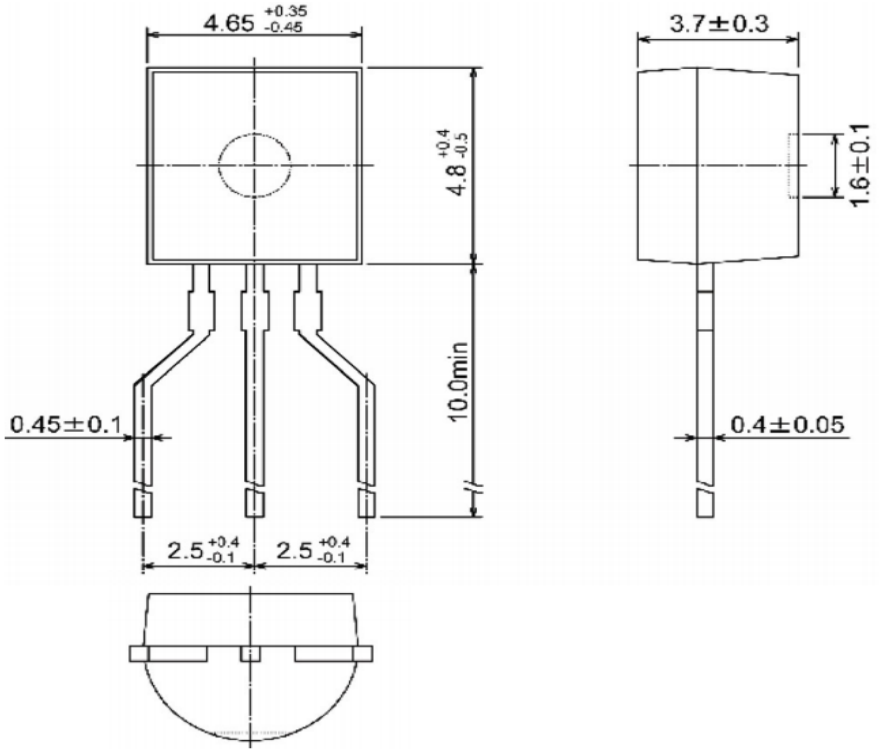
● **SOT89-3**




● **SOT23-3**



● **TO-92**


4.65 +0.35 -0.45
3.7±0.3
4.8 +0.4 -0.5
1.6±0.1
10.0min
0.45±0.1
0.4±0.05
2.5 +0.4 -0.1
2.5 +0.4 -0.1