Tips for PCB Vias Design

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Basic theory

Vias are often part of the signal routing. They are vertical connections between layers to simplify trace routing around other components or when there is a high density of interconnections to be made (i.e. BGA,μBGA). As PCB trace, the PCB vias also have an associated parasitic capacitance, inductance and impedance. These parasitic values can be calculated as follow:

Capacitance: $C=1.41\times\varepsilon\times T\times D1/(D2-D1)$ [1]

Inductance: $L=5.08h\times [\ln(4H/D1)+1]$ [2]

where ε is the relative dielectric constant of PCB, D1 is the diameter of the via, D2 is the diameter of the anti-pad, T is the thickness of the PCB, and H is the length of the via.

Take a 1.6mm FR4 PCB (ε=4.4 below 500Mhz) as a example, one 10mil/20mil via will add $C=1.41\times4.4\times0.067\times0.02/(0.04-0.02)=0.42pf$ capacitance and $L=5.08\times0.067\times[\ln(4\times0.067/0.01)+1]=1.46nH$ inductance to the trace.

These added capacitance and inductance will have the effect of more time delay, longer rise and fall times of the signal, degrading signal integrity. This maybe not a problem at lower frequencies designs. However, it could become a critical issue in high speed printed circuit board design.

Vias can also cause a step-function change in trace impedance. A typical value of the impedance drop on the via is about 10% (this could be variable depends on the via's size, pcb thickness, etc.,). Take a 50ohm trace as example, the reflection coefficient is (50-45)/(50+45)=5%. As most high speed designs do not carry more than several mA, the impact of via impedance is not vital as the capacitance and inductance does.

Case study

To estimate the signal integrity effects of Vias, two micro-strip lines in a typical 4-layers PCB are been studied.

Modelling:

PCB thickness	1.6mm	**Copper weight**	Top & bottom: 1oz; Inner layers: 0.5oz;
Stack-up	Top (signal), GND,PWG, Bottom (signal)	**Driver**	CMOS 3.3V output
Material	FR4, ε= 4.4 (below 500Mhz)	**Receiver**	CMOS 3.3V input

Table 1 Simulation Setup

Net 1:

U1.1 and U2.1 are connected with 2.5 inches micro-strip trace, which the characteristic impedance is 51.8ohm. 50 ohm resistors are serial connected at U1.1 side as source termination.

Net 2:

Five of serial connected half inch length traces are routed between U3.1 and U4.1. Four 10mil/20mil vias are placed between these traces. The total trace length between U3.1 and U4.1 is the same as the length between U1.1 and U2.1 (see below figure).

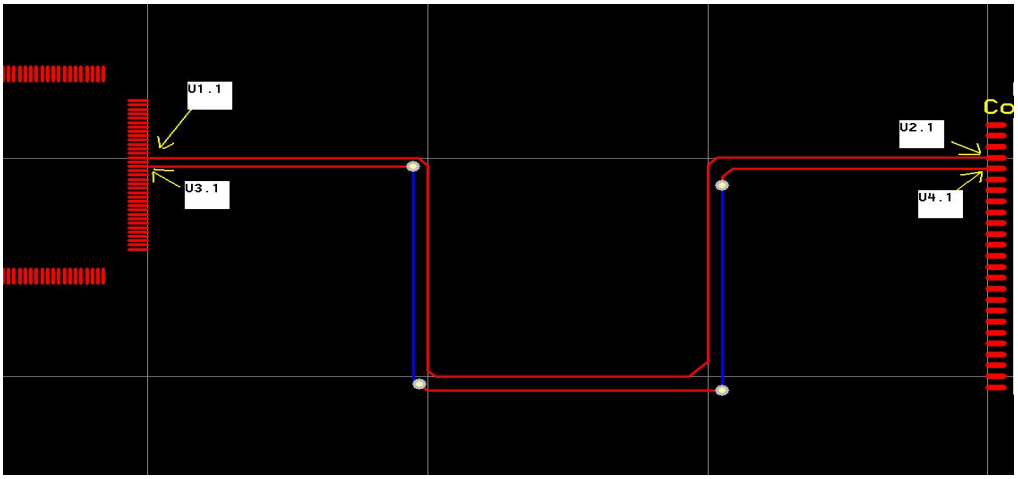

Figure 1 Two micro-strip lines

Both nets were created with IBIS models as below for simulation.

Net1:

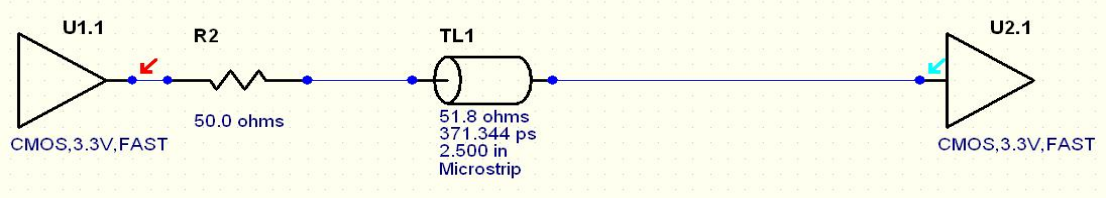

Figure 2 Trace without via

Net 2:

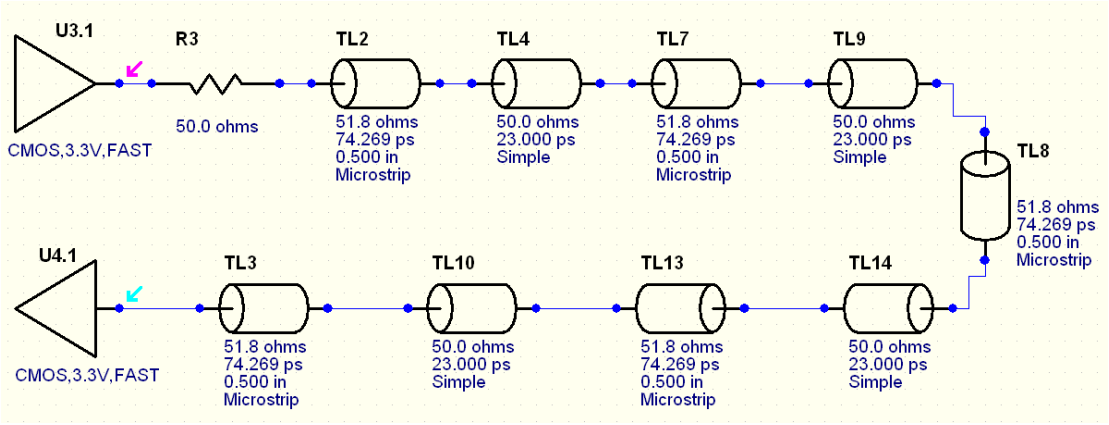

Figure 3 Trace with Vias

Simulation analysis

Simulations are performed using Hyperlynx™ Linesim from Mentor Graphics. The simulated signal frequency is 400Mhz and the signal slew at the driver side is 400ps. High impedance probes were placed on the pins of U1.1,U2.1, U3.1 and U4.1. The time domain parameters were analyzed. The followings are the rise and fall edge waveforms.

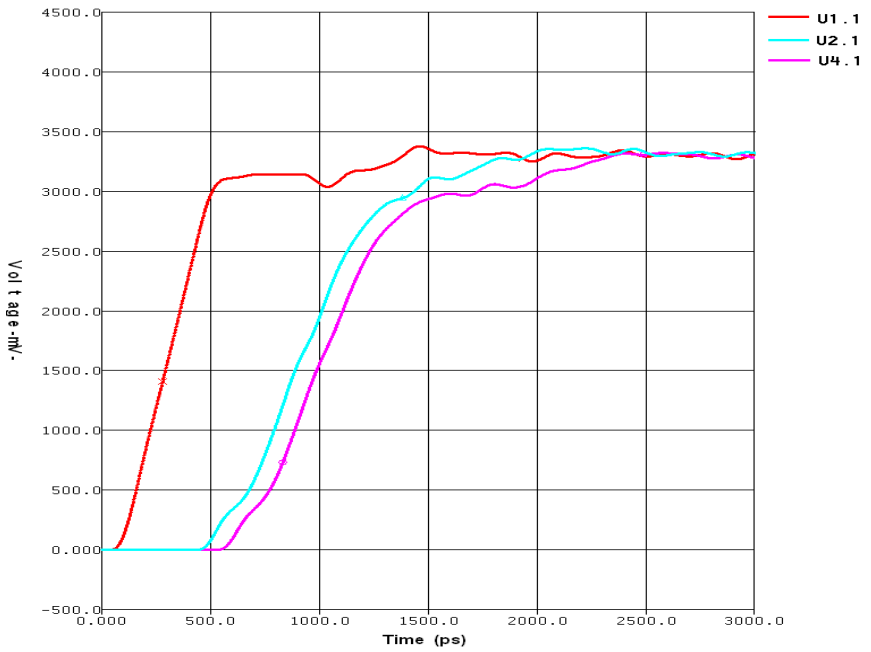

Figure 4 Rising edge waveform

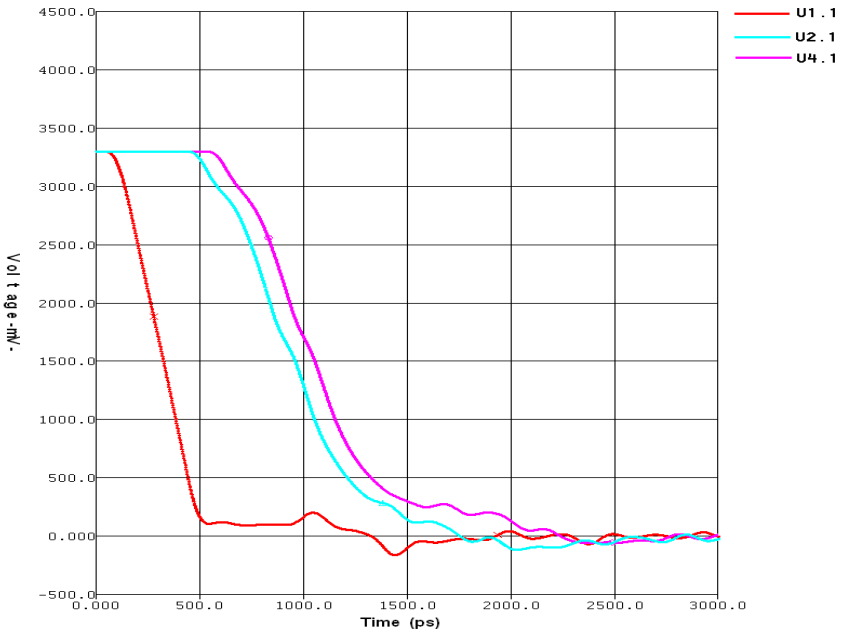

Figure 5 Falling edge waveform

Probe position	Delay (checked at 10% of rising edge)	Rising time (10%to 90%)	Falling time (10%to 90%)(ps)	Signal bandwidth (BW=0.35Tr)
U1.1	134ps	376ps	341.5ps	931Mhz
U2.1	446ps	857ps	765.5ps	408Mhz
U4.1	550ps	1054ps	817ps	332Mhz

Table 2 Time domain parameters

Net 1 is a single 51.8 ohm transmission line. A 376ps rise time single trigged on U1.1, by 312ps the signal reaches U2.1, the rise time degraded to 857ps due to the parasitic on the transmission line.

Exactly the same length of the line on net 2, however the rise time on far end degraded to 1054.1ps, 192ps further than net 1. The main factor contributing to this downgrading is coming from the added vias. Clearly, the via between traces negatively affects the single waveform.

To further analysis the impacts of the vias on the trace, different numbers of the vias (2,3, and 4) and different size of vias (10/20mils and 20/40mils) are simulated on Net 2. Results are summarized as below:

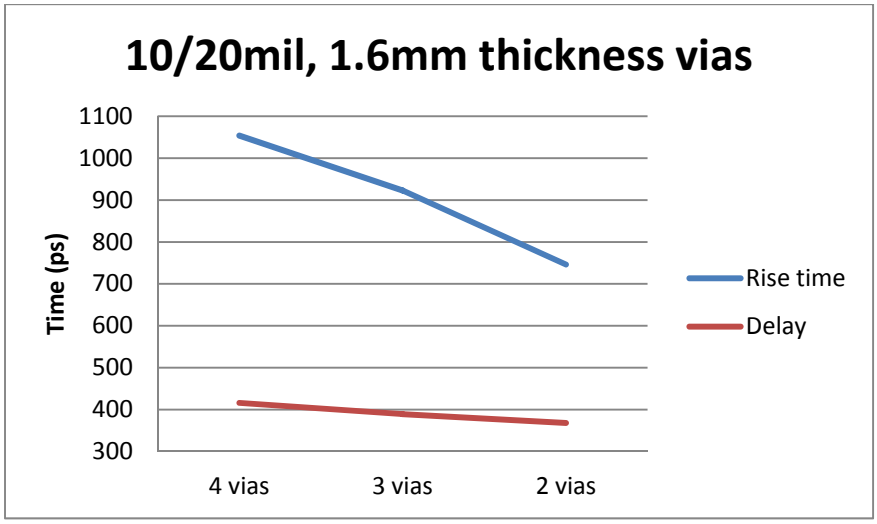

Figure 6 10/20mil,1.6mm length vias, tested at U4.1

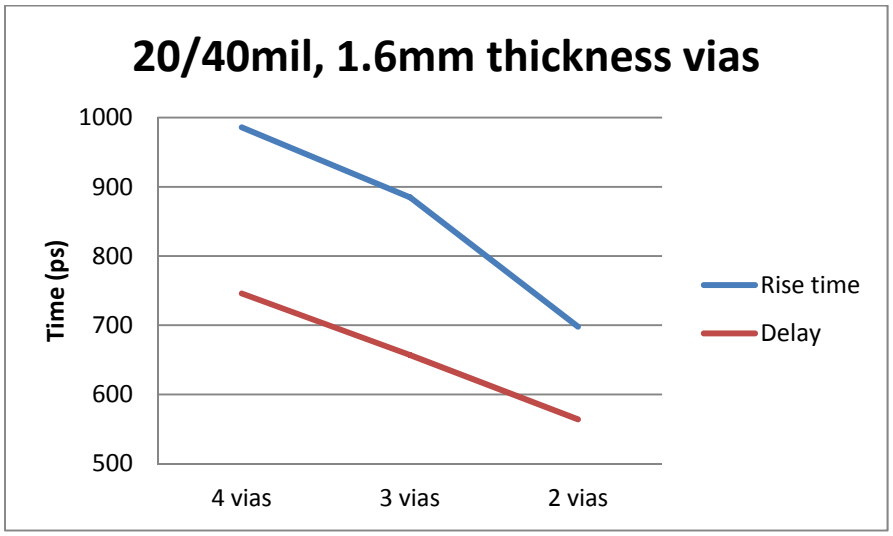

Figure 7 20/40mil,1.6mm length vias, tested at U4.1

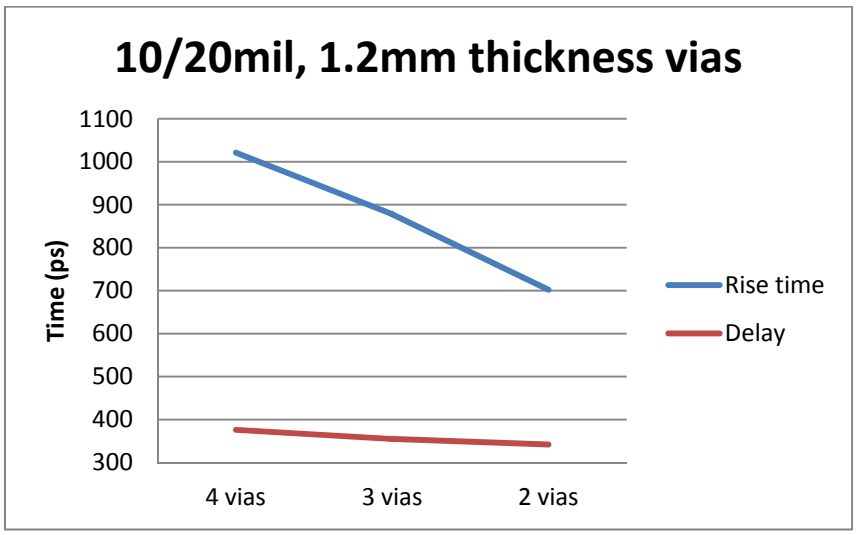

Figure 8 10/20mil,1.2mm length vias, tested at U4.1

The above simulation result shows:

1.Less number of the vias on the trace results in shorter delay and quicker rise time.

2. Smaller vias can get less delay, but not significantly decreasing on the rise time.

3. keeping the length of via shorter can get less delay and quicker rise time.

Be noted the above summary is not always right as the trace/via geometry maybe widely varied in the real circuits. However most complicated topologies can be decomposed as the combination of many *trace + via + stub* elements. Pre-layout simulation with EDA tools is always a helpful way to analysis the critical signals before PCB routing.

Practical guidelines:

The following via design guidelines using in PCB design process are recommended to enhance the engineering performance, saving cost, increasing the stability of the products.

Vias in high speed circuit design

1. Avoid using vias and layer changes if possible to avoid signal distortion.
2. Do not use via in high frequency clock transmission line.
3. When possible, remove any unnecessary pads on vias because these pads create parallel plate capacitance.
4. Smaller vias have lower capacitance. Short length, larger diameter vias have lower inductance. Both parasitic elements can have detrimental affects, but it is often the parasitic inductance element that provides an unexpected series impedance that creates signal transmission problems.
5. Keep the number of vias of the two differential traces the same to minimize the skew and phase difference.

Power/ground vias

For signal net, the bottleneck for the current carrying capacity is not on the via. Check the capacity on the trace (line) to get the maximum carrying capacity for the entire net.

For power net, the bottleneck is on the via, the following are some thumb of rules:

10/20mil vias with 0.5oz copper weight, the maximum safety current is 0.5A.

10/20mil vias with 1.0oz copper weight, the maximum safety current is 0.75A.

20/40mils Vias with 0.5oz copper weight, the maximum safety current is 0.95A.

20/40mils Vias with 1.0oz copper weight, the maximum safety current is 1.25A.

For other size or type vias, the current capacity can be estimated by equivalent trace capacity, where the trace width can be calculated by: diameter*3.14*0.6. For example, a 20mils via is effectively a 37.7mils width trace on the current carrying capacity.

Thermal vias:

1. Increase plating thickness of the vias where possible to keep the thermal resistance minimum.
2. Increasing the pad size of the vias is an inexpensive way to improve the thermal spreading capacity.
3. Placing multiple small vias evenly at high power dissipation area can improve the overall thermal transfer ability comparing with one big via.
4. Vias may become filled with the solder during reflow process, this will result in less effectively of heat spreading.
5. Making solid vias, which thermally conductive material filled into them, can get lower thermal resistance. However, this adds an additional step in PCB production so extra cost will be applied.
6. Buried/blind vias have higher thermal resistance comparing with the same dimension through hole vias.

Other general rules

1. Blind/buried vias are smaller and act less as a discontinuity in HDI design. However, the typical PCB manufacturing cost for using blind/buried via technologies is 12% higher comparing with the same configuration PCBs which only using the normal through hole Vias (based on Quick-teck 2012 PCB cost analysis report).
2. Place power/ground via near power supply pins of IC, so get the power supply path short.
3. Add ground vias nearby the area where high speed signal changes layer. This allows the return current flow near to the signal current flow, adding positive impact on EMI and signal integrity.
4. Via-in-pad design is better thermally than normal pad, but it could be the reason of pseudo soldering in the reflow soldering process.
5. For BGA and µBGA solder joints, it is suggested to use filled via if Via-in-pad design have to be accomplished.
6. High density vias can negatively affect the PCB mechanical performance. PCB twist/wrap check is recommended on this area.